FILED UNDER 35 U.S.C. 371

PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

**APPLICANTS: Eder Stefan; **CONTINUING DATA VERIFIED: THIS APPLICATION IS A 371 OF PCT/DE00/01737 C5/29/2000 QK . BU. **FOREIGN APPLICATIONS VERIFIED: GERMANY 199 25 422.2 06/02/1999	APPL NUM 10089425	FILING DATE 07/29/2002	CLASS SUI	BCLASS	GAU 2836	EXAMINER
THIS APPLICATION IS A 371 OF PCT/DE00/01737 C5/29/2000 OK. PSV. BEST AVAILABLE COPY "FOREIGN APPLICATIONS VERIFIED: GERMANY 199 25 422.2 06/02/1999 C. L. PV. PG-PUB DO NOT PUBLISH RESCIND Proeign priority claimed Styes no ATTORNEY DOCKET NO Styes no Reyes no Re	**APPLICANT	S: Eder St	efan;	<u> </u>	<u> </u>	
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TITLE: Circuit comprising an integrated switching circuit and a voltage regulating circuit U.S.DEPT. OF COMM./PAT. & TM-PTO-436L(Rev. 12-4				ng circuit a	ind a volta	ge regulating circuit U.S.DEPT. OF COMM/PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED			
	Assistant Examiner	Total Claims		Print Claim for O.G	
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Amount Due Date Pald		Sheets Drwg.	Figs.Drwg.	Print Fig.	
AND CONTRACTOR OF THE STATE OF	Primary Examiner				
TERMINAL	PREPARED F R ISSUE	Application	Examiner	ના કામ સ્થેતિ કરી. -	
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